13.4 A 5th-order CT/DT Multi-Mode ΔΣ Modulator

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With the advent of new cellular communication standards like UMTS and the large install-base of current standards like GSM, mobile devices capable of working in different modes are desirable. In order to support multiple modes, a reconfigurable receive chain is the preferred option to minimise total silicon area. Because of the potential for low power consumption and inherent anti-aliasing behaviour [1], a CT ΔΣ ADC is often preferred for the digitization of the analog baseband signal in a receive chain [2]. Disadvantages of the CT implementation are the dependency of the loop-filter parameters on the RC product and the sensitivity to clock jitter [1]. The large processing spread on the RC product can shift the position of the poles and zeros of the noise transfer function (NTF). To prevent in-band quantisation noise to become too high, the loop filter components can be tuned, requiring an RC-product measurement circuit. The NTF of a DT implementation (e.g. SC) does not suffer from process variations as its parameters are dependent on the clock frequency and component ratios. The disadvantages are the large current necessary for fast settling and the need for an anti-aliasing filter [3]. The design proposed in this paper offers the accurate loop-filter parameters of a DT loop filter while retaining (some) anti-aliasing behaviour at current levels similar to a CT implementation. The multi-mode ADC converts EDGE/CDMA/UMTS baseband signals, achieves 88/82/73dB DR, and is designed for embedding in a 65nm CMOS SoC. It draws less than 1.5mA from a 2.5V supply.

The block diagram of the ΔΣ ADC is shown in Fig. 13.4.1. The 5th-order loop filter is a combination of CT and DT: the 1st integrator is a CT opamp RC integrator as in [1, 4], the 2nd to 5th integrator are DT OTAs loaded with capacitors. Feedback capacitor C_3 and OTA B_5 each implement 1 notch in the NTF (CDMA and UMTS mode only). In EDGE mode the 5th stage is not used to reduce the capacitor area and no notches are present. The feedforward coefficients (CT OTAs) provide a current domain signal to the comparator which in turn delivers the output bit stream. For reduced jitter sensitivity the feedback DAC is of the SC type [4]. All capacitors are gate-oxide capacitors. The clock frequencies for the EDGE/CDMA/UMTS modes are 26, 76.8, and 153.6MHz, respectively.

From the location of the feedforward coefficients (after the 1st integrator) and the use of a 1b quantizer, it can be concluded that the unity-gain (UG) frequency of the 1st integrator does not influence the NTF. The NTF is determined by the 2nd to 5th stage, the feedback coefficients, and the feedforward coefficients. The spread on the UG frequency of the 1st integrator due to the RC combination influences the maximum input signal. Internal signal levels in the loop filter are dependent on the feedback capacitor of the 1st integrator, the DAC capacitor and the reference voltage.

Figure 13.4.2 shows the signal levels after the CT 1st integrator. Because of its low-pass characteristics, in-band signals are amplified while high-frequency aliasing components are suppressed. Overall alias suppression is the ratio between the 1st-integrator in-band gain and its attenuation of the aliasing components.

Figure 13.4.3 shows the DT OTA, a differential pair degenerated with a SC network. When the settling is complete the OTAs transconductance is a function of the clock frequency and C_{deg}. Because there is no feedback loop (as in traditional SC circuits [3]) there are no stability issues and settling can be fast. Due to the 2-phase switching, the 1st aliasing components originate from the band around twice the clock frequency. Aliasing, however, also occurs from the band around the clock frequency, this due to the finite transconductance of the opamp in the 1st integrator and the time-varying output impedance of the SC DAC.

The comparator shown in Fig. 13.4.4 is designed for high bandwidth, fast settling, and rail-to-rail output signals. When the clock signal is low, the input signal (a differential current) generates a differential voltage on the sources of transistors MN_0 and MN_1 (charge difference on C_{gs} of the transistors). When the clock signal goes high, the sources of MN_0 and MN_1 are connected to ground. The C_{gs} charge difference generated during the previous clock phase now results in a gate voltage difference. The combination of MN_0, MN_1, MP_0, and MP_1 forms a gain stage that amplifies the voltage difference to a rail-to-rail output signal. Initially the high current in the amplifier gives it a very high bandwidth, but after settling, the amplifier no longer consumes current.

The circuits of the ADC are designed with PSRR and substrate noise in mind. All signal processing is done in differential circuits with the common-mode level related to the substrate. This allows the use of both NMOS and PMOS (Nwell never to V_{DD}) transistors for signal processing. To reduce the substrate noise the digital circuits are placed in a separate Pwell isolated from the P-bulk material by a deep Nwell. In this way the Nwells of the analog PMOS transistors do not need to be connected to V_{DD}. The 2.5V design is implemented in a 65nm CMOS process using thick-oxide transistors and is part of a larger mixed-signal chip including a reference circuit, PLLs, decimation filters, and various audio blocks . The area for the converter including reference buffer is 0.125mm^2.

Figure 13.4.5 shows the output spectra for the intermodulation measurement for EDGE and UMTS. Note that the visible 2nd- and 3rd-order harmonic signals originate in the signal sources, only the intermodulation is caused by the ADC [4]. The measured specifications of the ΔΣ ADC are summarized in the table in Fig. 13.4.6. Measured DR is 88/82/73dB for EDGE/CDMA/UMTS, respectively, while the power consumption is 2.6/3.1/3.7mW (including reference buffer). The increase in power consumption when increasing the clock frequency is caused by the higher power consumption of the digital circuitry. Note also the difference in aliasing behaviour around once and twice the clock frequency: this difference can be contributed to aliasing mechanism of the SC OTAs as described earlier.

References:

[1] E.J. van der Zwan, E.C. Dijkmans, "A 0.2 mW CMOS ΔΣ Modulator for Speech Coding with 80 dB Dynamic Range ," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1873-1880, Dec., 1996.

[2] P.G.R. Silva, L.J. Breems, K.A.A.Makinwa, et al., "An 118dB DR CT IF-to-Baseband ΔΣ Modulator for AM/FM/IBOC Radio Receivers," *ISSCC Dig. Tech. Papers*, pp. 66-67, Feb., 2006.

[3] R. Gaggl, A. Wiesbauer, G. Fritz, et al., "A 85-dB Dynamic Range Multibit Delta-Sigma ADC for ADSL-CO Applications in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1105-1114, Jul., 2003.

[4] R. van Veldhoven, "A Tri-Mode Continuous-Time ΔΣ Modulator with Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver," *ISSCC Dig. Tech. Papers*, pp. 60-61, Feb., 2003.

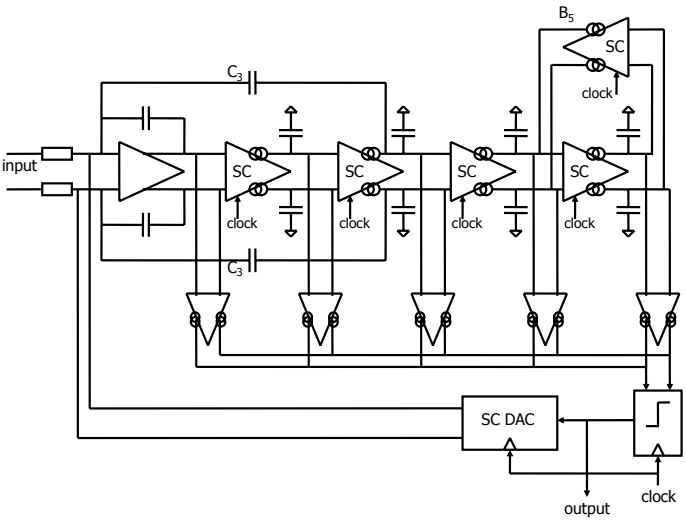

Figure 13.4.1: Block diagram of the modulator.

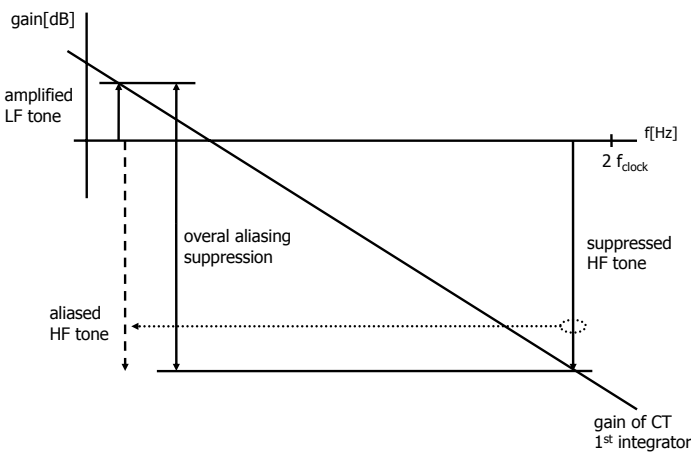

Figure 13.4.2: Alias suppression.

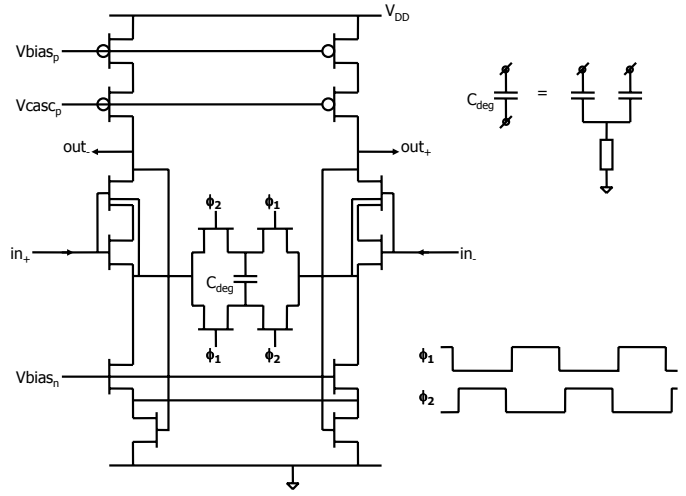

Figure 13.4.3: Switched-capacitor OTA.

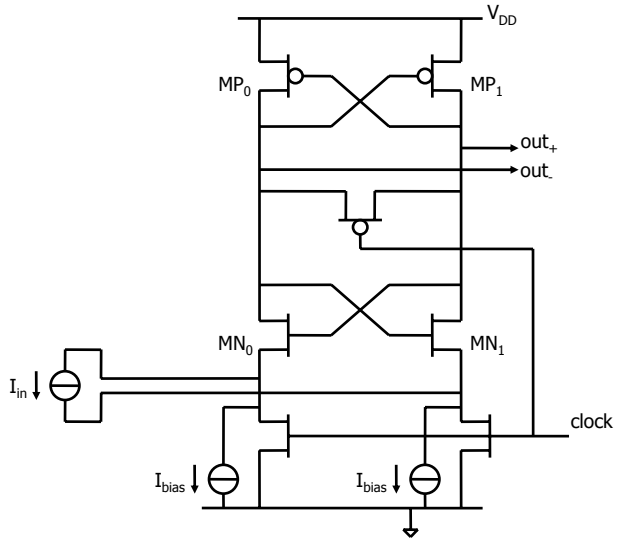

Figure 13.4.4: Comparator.

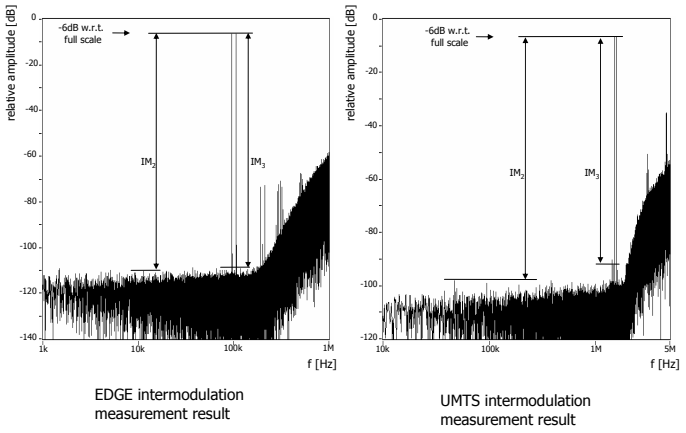

Figure 13.4.5: Intermodulation measurement results.

	EDGE	CDMA	UMTS
DR [dB]	88	82	73
IM_2 [dB]	> 98	> 91	> 82
IM_3 [dB]	> 98	> 91	> 86
Clock frequency	26MHz	76.8MHz	153.6MHz
Alaising suppression, f_{clock} [dB]	-52	-48	-41
Aliasing suppression, 2 f_{clock} [dB]	-46	-	-
Power consumption	2.6 mW	3.1 mW	3.7 mW
FOM	470fj/conv	250fj/conv	260fj/conv
Bandwidth	135 kHz	614 kHz	1.92 MHz
Order of ΔΣ	4	5	5
Process	65nm CMOS		
Area	0.125mm^2		
Supply voltage	2.5V		

Figure 13.4.6: Measured specifications.